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Electro-Thermal Simulation of Multi-channel Power Devices on PCB with SPICE

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Abstract

In this paper we will present an efficient method allowing thermal modeling, simulation and design of a multichannel power semiconductor device on Printed Circuit Board (PCB). The method starts with a finite element discretization of the heat equation at the continuous field level. In a second step, the resulting large set of differential equations is approximated by a reduced-order model by means of the well-known Arnoldi algorithm. Next, the reduced-order thermal model is represented by an electrical equivalent network allowing SPICE simulation. The new approach allows to simultaneously evaluate the temperature of the semiconductor junctions and of the PCB track underneath the semiconductor device.

The entire model generation procedure was automated and is now available for use with the software tool ANSYS/Workbench. This allows the development of a set of thermal SPICE models of different devices and different PCB design layouts. We will demonstrate the method by performing an electro-thermal analysis of Freescale's new eXtreme Switch devices. These devices typically consist of 4 high-side MOSFET switches with associated drive-, diagnostic- and protection circuitry integrated in a Power Quad Flat No-Lead (PQFN) package. A typical application demonstrates the validity of the followed approach.

1. Introduction

It is important to keep the maximum junction temperature of a MOSFET power die within the authorized range. Otherwise overheating will impact the reliability and cause device failure. On the other hand, the PCB surface, used as a heat-sink, must be minimized to save costs. Hence, the ability to predict the thermal performances of a particular design layout is a crucial element when a cost-optimized and reliable system must be designed. In this paper we will present an efficient modeling method for design and simulation of multichannel power semiconductor devices in a realistic applicative environment. We start with a full scale finite element model (see Section 2), and then introduce the model order reduction (see Section 3). That allows us to reduce the complexity of the original final element model and makes it possible to go to system level simulation. In section 4 we will briefly describe the transformation of the state space representation of the dynamic heat equation into an electrical equivalent circuit, represented by a SPICE netlist. The entire system and the simulation of selected application cases, including electro-thermal coupling, will be shown Section 5.

2. Finite Element Modeling

The most accurate thermal model is generally achieved by means of finite element modeling, but this approach is much too time consuming to allow an interactive design optimization. Here the original geometry is replicated in the model where additionally the thermal properties of each part are specified. Figure 1 shows pictures of the eXtreme Switch device. The PQFN package is a Multi Chip Module (MCM), which carries one control- and one power die interconnected through copper leadframe, heavy gauge aluminum and gold bonding wires. During module assembly, the PQFN pads are soldered onto a printed circuit board. Figure 2 shows the associated solid model as introduced in a CAD-tool.

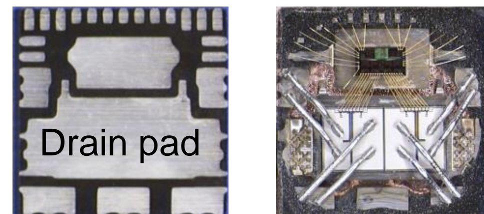

Fig.1: Semiconductor package, left: bottom view with exposed pads, right: top view of a de-capsulated package

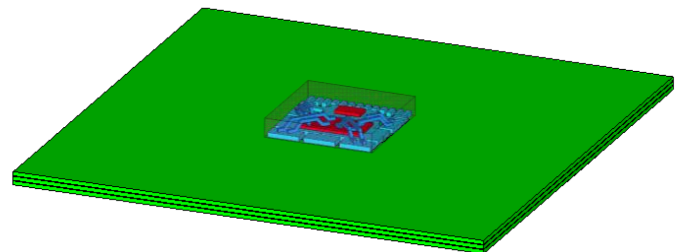

Fig. 2: Solid model of the assembly of package and PCB

During finite element meshing the solid model is divided into a finite number of elements (see Fig 3). The partial differential equation for transient heat conduction reads

$$\nabla k \nabla T + Q - \rho C \frac{\partial T}{\partial t} = 0 . \qquad (1)$$

With the finite element discretization Eq (1) is replaced by the following set of ordinary differential equations:

$$\mathbf{H} \cdot \dot{\mathbf{T}} + \mathbf{K} \cdot \mathbf{T} = \mathbf{F} \cdot \mathbf{p_J} , \qquad (2)$$

where the matrices **H**, **K** and **F** represent heat capacity, thermal conductivity and load distribution. Vectors **T** an $\mathbf{p_J}$ represent all nodal temperatures and the heat dissipation power in the particular transistor junctions.

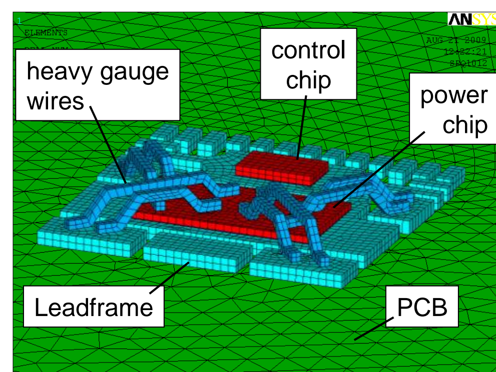

Fig. 3: Finite element mesh (mold compound removed).

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Eq (2) could be directly converted to a Kirchhoff-network consisting of thermal resistors and capacitors [1]. But, by the nature of the finite element method, the dimension of such a model would become rather high. For example, the number of degrees of freedom of the model in Fig 2 would approach 300 000 and is out of reach for effective representation by an electrical equivalent circuit.

There are many ways to develop a compact dynamic thermal model [2][3] but in our view model order reduction [4][5][6] possesses the most attractive properties.

3. Model Order Reduction

The model order reduction is based on the assumption that the movement of a high-dimensional state-vector can be well approximated by a small dimensional subspace (Fig 5 left). Provided this subspace is known the original system can be projected on it (see Fig 5). The main question is how to find the low dimensional subspace that possesses good approximating properties. It happens that a very good choice is a Krylov subspace [4]-[6].

The model reduction theory is based on the approximation of the transfer function of the original dynamic system. It has been proved that in the case of Krylov subspaces, the reduced system matches moments of the original system for the given expansion point. In other words, if we expand the transfer function around the expansion point, first coefficients will be exactly the same, as for the original system. Mathematically speaking this approach belongs to the Padé approximation and this also explains good approximating properties of the reduced models obtained through modern model reduction methods. The description of the algorithm can be found in [4]-[6].

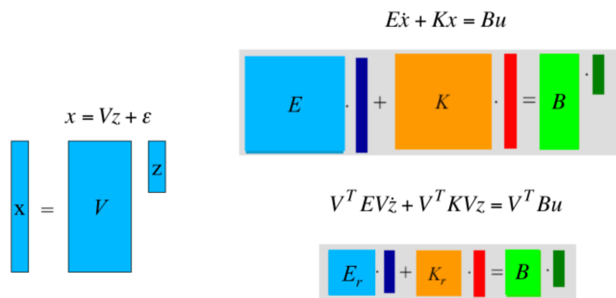

Fig. 5: Model reduction as a projection of the high dimensional system onto the low-dimensional subspace.

The reduced low order system is given as a state space representation of the transient heat equation with the state vector of generalized variables $\mathbf{z}$, the evolution matrices $\mathbf{E}$ and $\mathbf{A}$, the input matrix $\mathbf{B}$ and the output matrix $\mathbf{C}$. The vector $\mathbf{T_J}$ comprises all transistor junction temperatures. The required number of state variables is determined by an error estimation procedure [7].

$$\begin{aligned} \mathbf{E} \cdot \dot{\mathbf{z}} &= \mathbf{A} \cdot \mathbf{z} + \mathbf{B} \cdot \mathbf{p_J} \\ \mathbf{T_J} &= \mathbf{C} \cdot \mathbf{z} \end{aligned} \qquad (3)$$

The software tool "MOR for ANSYS" [5] has been used to perform model reduction on the finite element models developed in ANSYS Workbench. The block scheme of the software is shown in Fig 6.

The software reads system matrices from ANSYS FULL files, runs the order reduction algorithm and then writes the reduced matrices out. The process of generating FULL files in ANSYS Workbench is automated through scripting. The developer defines named selections to describe the power dissipations in the model. The script (so called a command snippet) takes them as arguments and then defines the inputs and outputs and generates the files necessary to run MOR for ANSYS. This way the process to generate the reduced model is fully automated. The time to generate the reduced model is comparable with that of the static solution and for the model in Fig. 3 it is about 100 s.

A comparison of one transient junction temperature response in ANSYS (dimension of the model about 300000) with the reduced model of the dimension 30 is shown in Fig. 7.

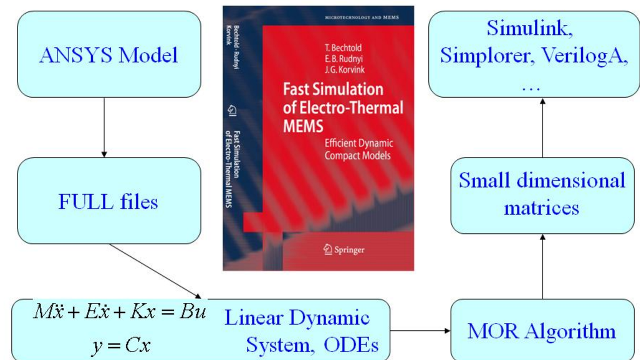

Fig. 6: The structure of MOR for ANSYS.

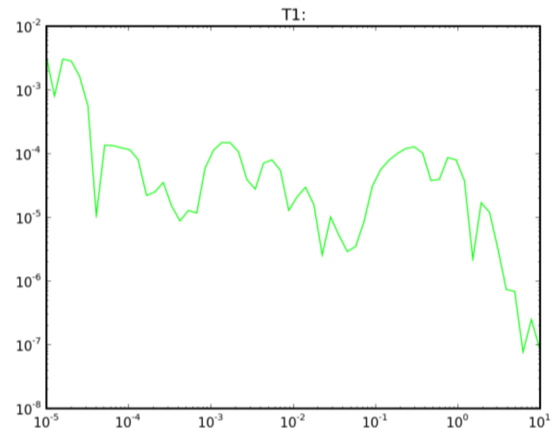

Fig. 7: The relative difference between the thermal response in ANSYS and that produced by the reduced mode.

4. Model Representation by an electrical equivalent circuit

The state space format is very common for data flow analysis tools. In system analysis it is handled as a dynamic block representing the heat transfer of a semiconductor package. Alternatively, the reduced system can be rewritten as an equivalent RC network model [6]. To achieve this, we diagonalize the state space matrices. The transformation matrix $\mathbf{U}$ is normalized such that the evaluation matrix $\mathbf{E}$ becomes an identity matrix. Each evolution equation can be replaced by one RC-cell with a unit capacitance and a resistance being the reciprocal of the associated diagonal element of evolution matrix**:**

$$\begin{aligned} \mathbf{U}^T \cdot \mathbf{E} \cdot \mathbf{U} &= \mathbf{I} \\ \mathbf{U}^T \cdot \mathbf{A} \cdot \mathbf{U} &= -\mathbf{Diag}\left(\frac{1}{R_1}, \frac{1}{R_2}, \cdots, \frac{1}{R_n}\right) \end{aligned} \qquad (4)$$

Input and output matrices $\mathbf{B}$ and $\mathbf{C}$ of the state space are now represented by controlled voltage_ and current sources. Fig. 8 shows a simplified thermal network model. The number of junction nodes was reduced to two for simplicity of the schematics.

The transformation of the reduced matrices in the form of Eq (4) to a SPICE netlist was automated through a Python script. The script reads the reduced matrices in the Matrix Market format produced by the MOR for ANSYS and then exports thus obtained subcircuit netlist.

As opposed to common CAUER- or FOSTER- type RC- circuits, the physical interpretation of the state space representation of the heat transfer presented here is not as obvious. The thermal state of the structure is completely described by the state vector. The evolution of each state variable in time is determined by the RC-cells. Heat sources (power dissipation) and resulting temperature readings are mapped by the controlled current and voltage sources. The state space model and its representation as SPICE netlist automatically includes all thermal cross couplings and multidimensional heat flow directions. This is a clear advantage for multichannel devices, such as Freescale's dual or quad analog power switches, where several power MOSFETs can be controlled independently by the user.

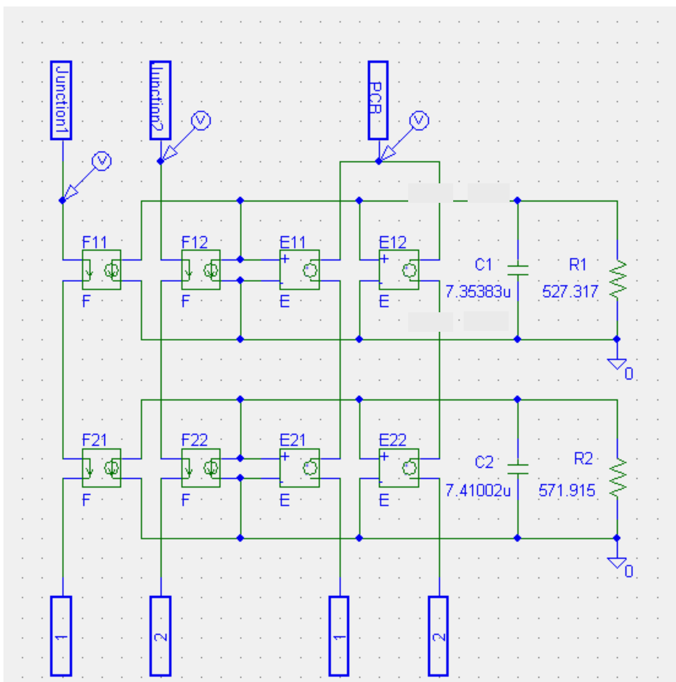

Fig.8: Electrical equivalent circuit representation of thermal state space model for multichannel devices (with exposed pad).

5. Thermo-Electric System Simulation

The proposed model generation path and electro-thermal system simulation are demonstrated for one of Freescale's new High-Side Switch devices with four independent channels. The device is packaged in the thermally well performing PQFN (Power Quad Flat No Lead) package. The corresponding thermal model contains two distinct submodels: one for the 4-Channel High Side switch and one for the associated printed circuit board (PCB). The device model provides the independent thermal ports, each of them representing the junction of one channel switch. Device model and PCB model share one common node, the voltage of which represents the temperature of the connection point between the device's drain terminal and the subjacent PCB land (see the drain pad in Fig. 9 and 10). The PCB model also represents the heat convection of the system into the ambient air.

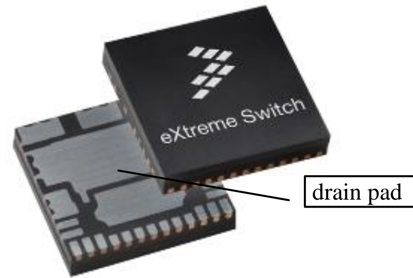

Fig. 9: an analog power IC (eXtreme Switch)

Two separate SPICE netlists were generated for the heat transfer in device and PCB. They are defined as simple sub circuits. The system model is easily done by importing the thermal subcircuits and the final assembly of thermal and electrical circuits. This can also be done with a schematics editor. The output node of the thermal device model is connected to the input node of the thermal PCB model (ref. Fig. 11). This approach allows to connect the PCB model of any other PCB layout to the same switching device just by replacing the associated SPICE sub circuit.

The system simulation is demonstrated for a power module that drives four bulb lamps with high inrush currents. All channels of the eXtreme Switch are connected to a 12V battery. Each output is connected to a bulb lamp.

The steady state load current level of one bulb is about 4A, whereas the maximum inrush current goes up to about 70A. The associated power dissipation is computed within each of the four high side power switch models, and fed into the corresponding terminals of the thermal device model.

The voltage at the four terminals of the thermal device model directly reflects the temperature within the particular transistor junctions. The drain pad node between device and PCB model reflects the average temperature of the drain terminal, which is equal to that of the PCB land to which the drain terminal is mechanically and electrically connected (ref. Fig. 11). Thermal cross-coupling between the channels is implicitly considered within the thermal device model. The ambient temperature is set to 85°C by means of a voltage source, which is connected to the thermal PCB model (ref. Fig. 11).

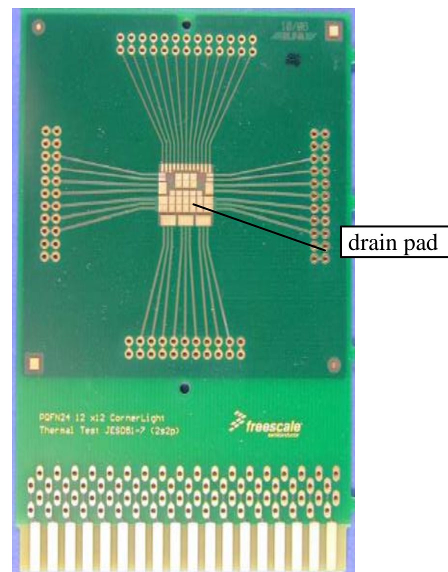

Fig. 10: Printed circuit board (here thermal test board 2s2p)

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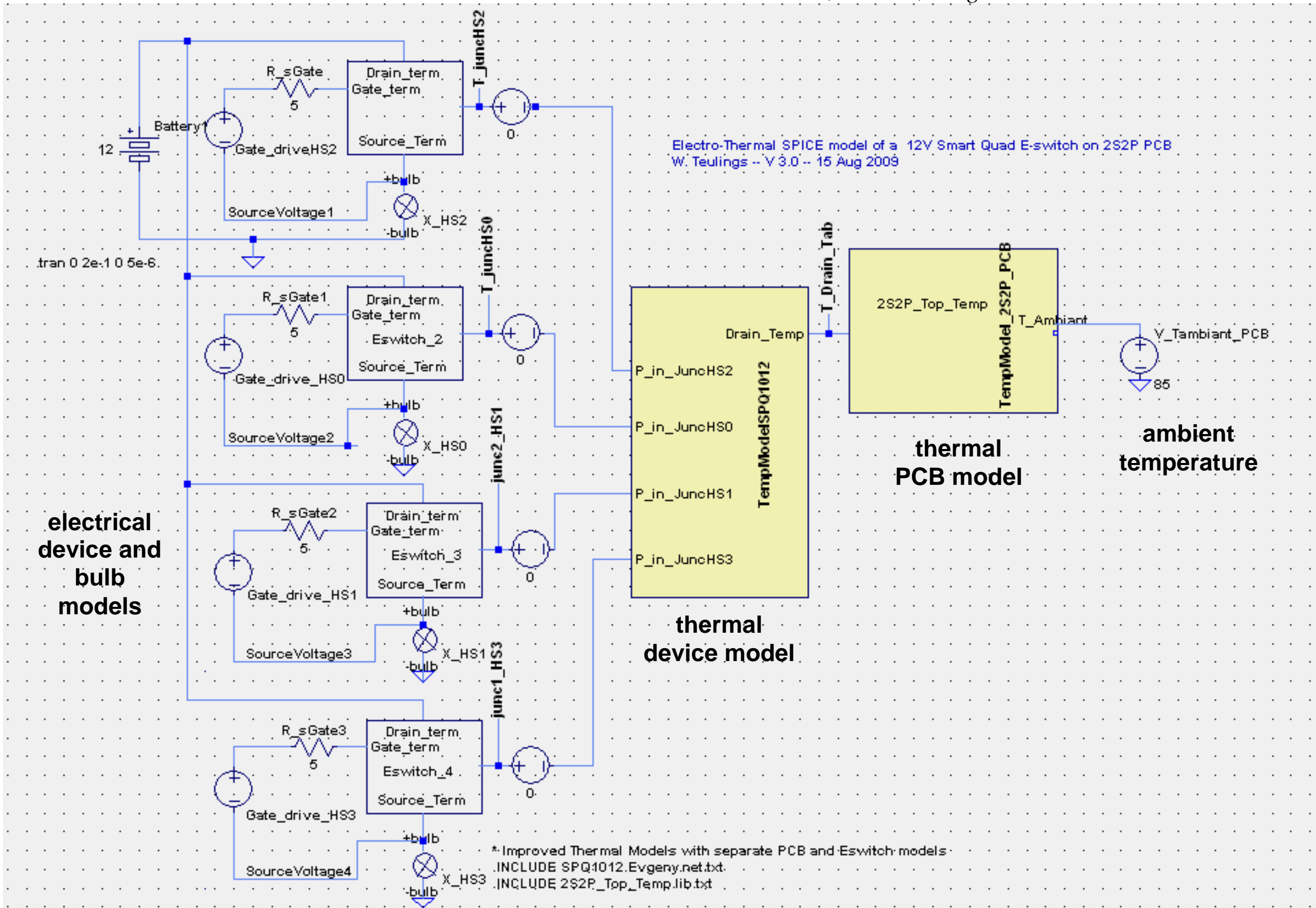

Fig. 11: SPICE circuit, with electrical equivalent circuit of the PCB and the 4 channel eXtreme switch device

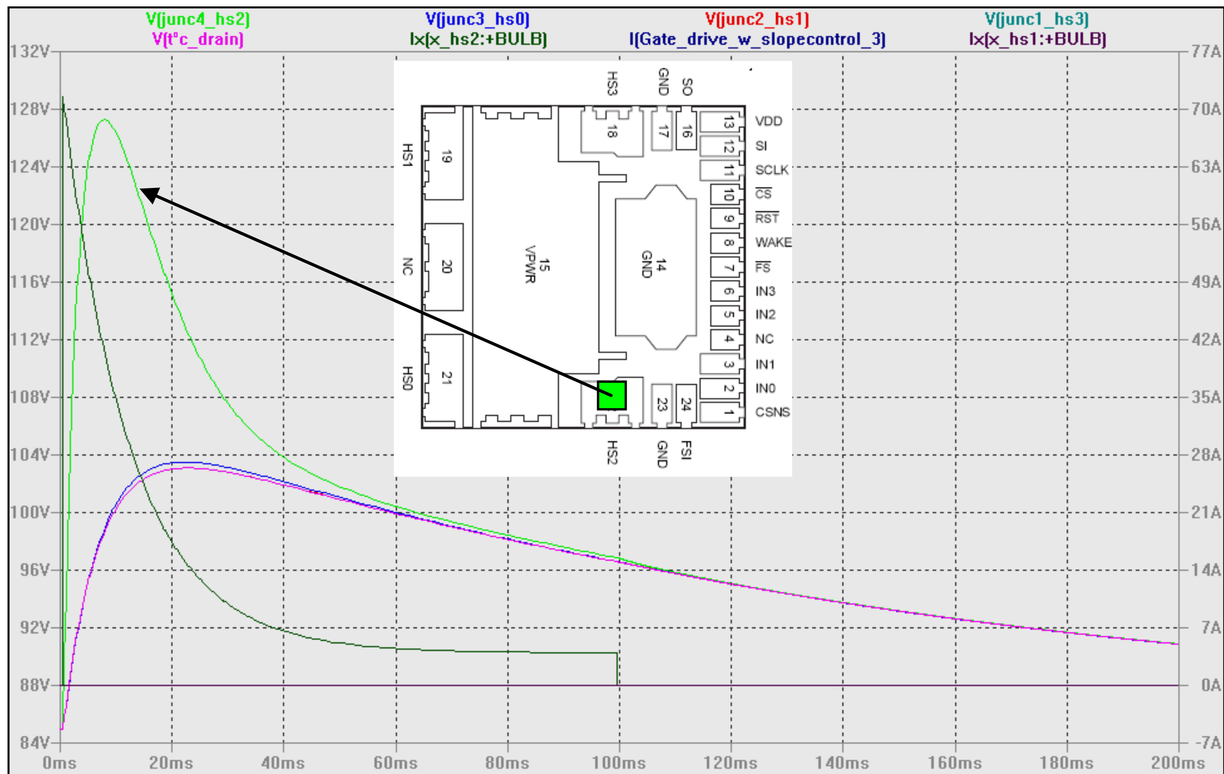

Fig. 12: Temperature response for use case 1, high side switch HS2 ON

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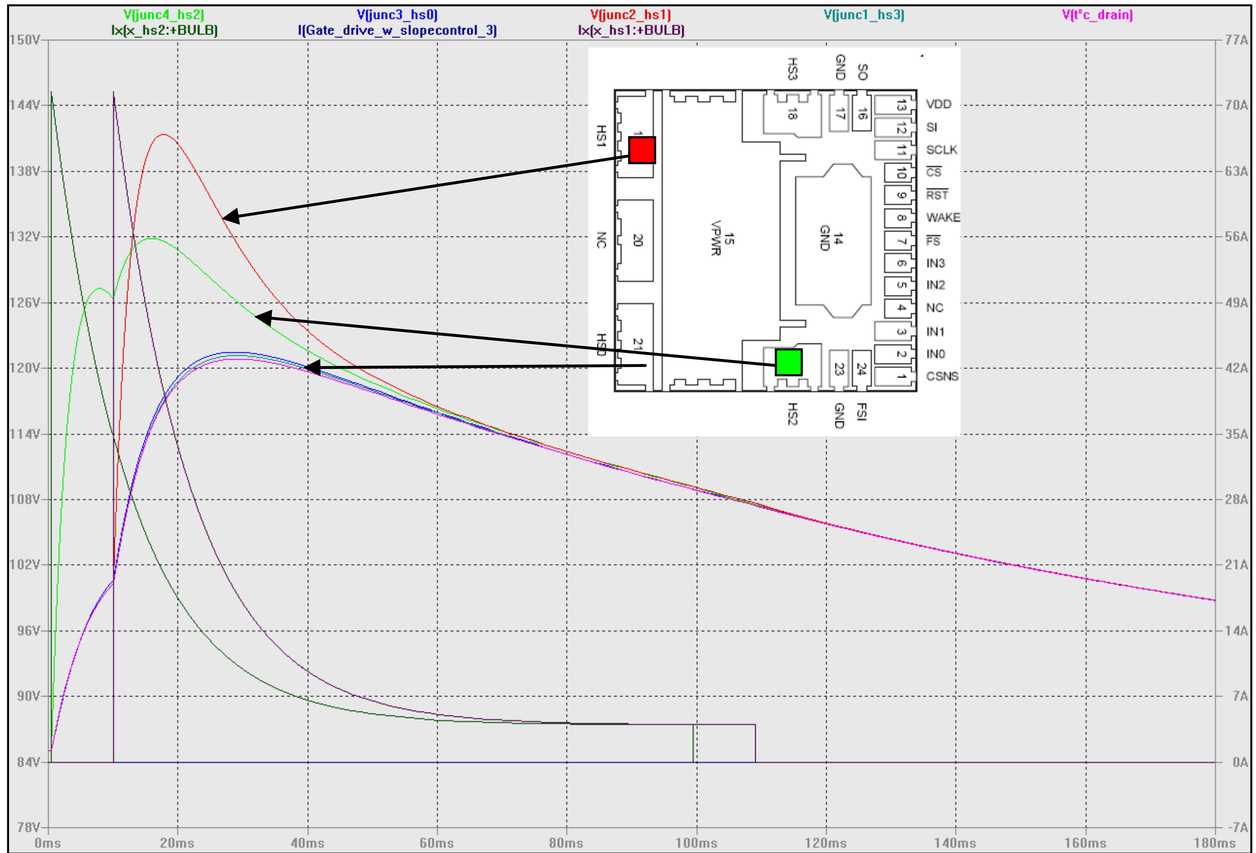

Fig. 13: Temperature response for use case 2, high side switches HS2 and HS1 sequentially switched ON

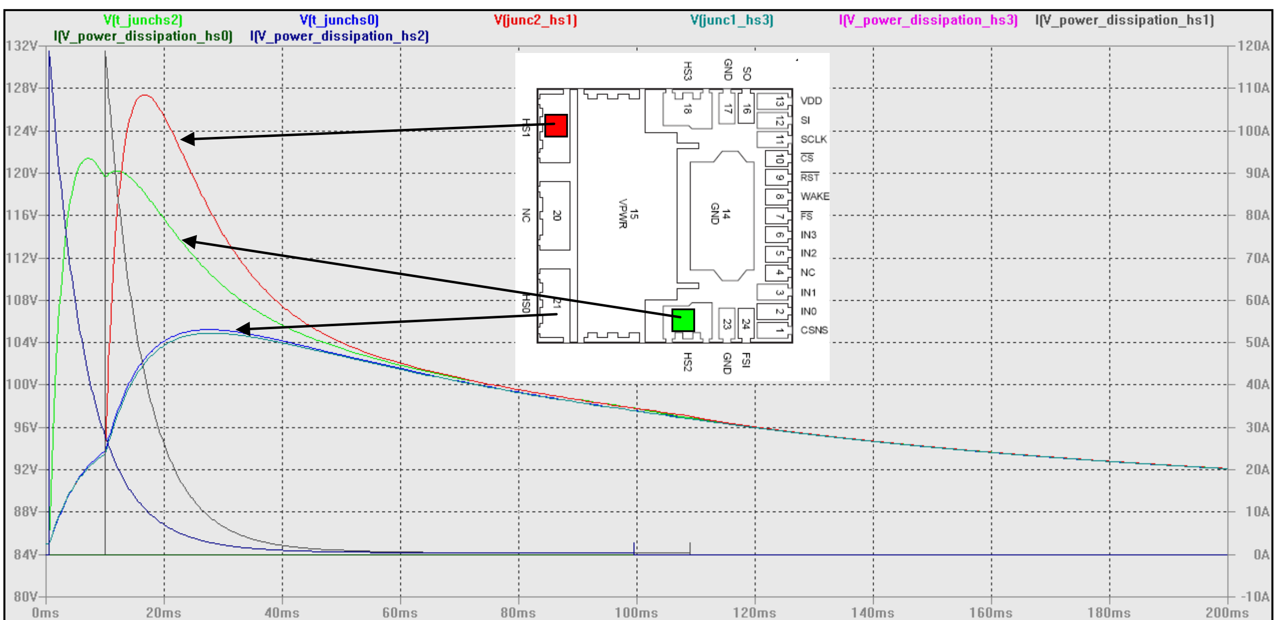

Fig. 14: Temperature response for use case 2 with the thermally enhanced printed circuit board

For the first use case, only the upper high side switch HS2 was switched on for 100ms. The inrush current peak only lasts a few milliseconds but reaches almost 70 Amps. Newt, the current exponentially decays to the nominal current load of 4 Amps. Figure 12 shows the resulting temperature response in transistor junctions and drain pad. It can be observed that channel HS2 (the only channel that carries current in this example) heats up to about 127°C. The other channels heat up to about 105°C due to cross-coupling (they do not dissipate any power themselves). Channel HS0, in closest proximity to HS2, heats up somewhat more than HS3 and HS1, as can be expected.

In a second use case the simulation has been repeated with an additional inner switch HS1 being put ON 10 milliseconds later than exterior switch HS2. It can be seen that first, the junction temperature of HS2 starts increasing as before. Next, after having started to decrease, it suddenly increases to a second maximum, due to cross-coupling induced by the power dissipation occurring in the adjacent switch HS1. The thermal cross coupling causes high side switch HS2 to heat up to 132°C. The temperature of high side switch HS1 reaches an even higher value of up to 141°C (ref. Fig. 13).

A third simulation run is repeating use case two but on a thermally enhanced printed circuit board lower thermal resistance). This time the maximum temperature of switch HS2 is significantly reduced compared to the previous simulation (ref. Fig. 14).

Freescale is able to supply SPICE models of several of its eXtreme switch devices for different PCB layouts. The combination of the component model with the PCB models is shown to be possible with the SPICE schematics editor. Thanks to this approach, system design with Freescale's eXtreme Switch devices will become very flexible and quick. It will enable our customers to cost-optimize their PCB layout and module design work without having to perform long, costly and tedious FEM simulations.

6. Summary

We presented a new procedure for thermal modeling& simulation of SMART power ICs (High Side Switches based on MOSFET) on Printed Circuit Boards with different layouts. Key elements were the order reduction of finite element models, the extraction of equivalent thermal circuit models, the assembly and simulation of electro-thermal systems with the circuit simulator SPICE. The proposed approach has many advantages:

- SPEED: A complete electro-thermal simulation with SPICE circuit simulator will take some tenth's of seconds, whereas any finite element simulation of a comparable system would take several hours,

- MODULARITY: Thanks to the separation of the thermal models of the device-package and that of the underlying PCB, the performance of several different PCBs may be evaluated within very short time. This allows a designer to fine-tune his design very quickly,

- FUNCTIONALITY: Coupling of electrical and thermal field becomes straight forward. Phenomena, such as the influence of an increased supply voltage on the power dissipation, may be evaluated by a simple SPICE simulation.

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