Electro-Thermal Simulation of Multi-channel Power Devices: From Workbench to Simplorer by means of Model Reduction

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Summary:

In this paper we present an efficient algorithm for the thermal simulation and design of multichannel power semiconductor devices. The simulation workflow starts with a finite element discretization of the heat transfer equation. In a second step, the resulting large system of differential equations is approximated with a reduced order model by means of the Arnoldi algorithm. The reduced order model is formulated as a state space representation suitable for the electro-thermal board/chip system analysis in a system simulation.

The entire modelling process is automated and is now available for use with ANSYS-Workbench and Simplorer. We will demonstrate the modeling flow for the electro-thermal analysis of new switch devices from Freescale. The application of the method is demonstrated for simulating dynamic thermal runaway.

Keywords:

Electro-thermal simulation, model order reduction, finite elements, system simulation, thermal runaway, dynamic compact thermal model, Simplorer, ANSYS Workbench, VHDL-AMS

1 Introduction

This work is a continuation of the paper presented recently at Therminic-2009 [1] where we have demonstrated the efficiency of model reduction for system level simulation. In this work we take the next step and report on how the new technology can be incorporated in the design flow with the use of tools from the ANSYS family.

We start with a short overview of the application of model reduction for thermal problems, then we review the main results from the previous work [1]. We then present the design flow with the use of ANSYS Workbench, MOR for ANSYS and Simplorer. Here another chip from Freescale will be used as a case study. Finally we describe the electro-thermal simulation with the reduced model in Simplorer where two different subsystems, thermal and electrical, are coupled with each other in a conservative manner using the VHDL-AMS behavioral modeling language.

2 Overview of Model Reduction

The partial differential equation for transient heat conduction [2]

$$\nabla k \nabla T + Q - \rho C \frac{\partial T}{\partial t} = 0 \tag{1}$$

combined with the convection boundary conditions

$$q = h(T - T_{bulk}) \tag{2}$$

is an efficient means to model thermal phenomena in a chip [3]. After the discretization of (1) and (2) by the finite element method one obtains

$$\begin{aligned} E\dot{x} + Kx &= Bu \\ y &= Cx \end{aligned} \tag{3}$$

where x is the state vector containing degrees of freedom in the finite element model, E and K are the heat capacity and heat conductivity system matrices. The load in Eq. (3) is presented in the form of a product of a constant input matrix B and a vector of input functions u that will represent the power dissipation in active devices as a function of time. The output vector y contains linear combinations of temperatures that are of interest in system level simulation, for example, the junction temperatures.

In terms of coupling this dynamic model to a system-level simulation, the classical state-space formulation is useful. Eq. (3) can be easily transformed into this form

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{4}$$

Eqs. (3,4) could be directly converted to a Kirchhoff network consisting of thermal resistors and capacitors [4] however the main problem along this route is that the state vector x is high dimensional. Consequently these equations are not directly applicable for system level simulation and a separate development of a dynamic compact thermal model is necessary [5].

Model order reduction [6] allows us to find a reduced model from Eq. (3) automatically. Its application to thermal problems has been documented, for example in [7]. The main assumption for model reduction is that the high dimensional state vector actually moves in a lower-dimensional subspace and we can project the original system on that subspace. As such, the goal of model reduction techniques is to find the low-dimensional subspace that accurately captures the dynamics of the state vector x.

For large systems the most efficient method to perform model reduction is implicit moment matching [7]. The idea of moment matching is to transform the dynamic system (3) into the Laplace domain and then to find such a lower-order system that has the same first derivatives in the Taylor expansion (moments) around some point as the original model. The direct implementation of this idea is numerically highly unstable. However, mathematicians have found that by means of the generation of a particular Krylov subspace, one finds such a projection subspace such that the reduced model matches the first moments [6] automatically.

The Arnoldi algorithm from [6][7] has been implemented in the software MOR for ANSYS (Fig. 1) that reads the system matrices directly from the ANSYS files, performs model reduction, and then writes the reduced matrices [8][9].

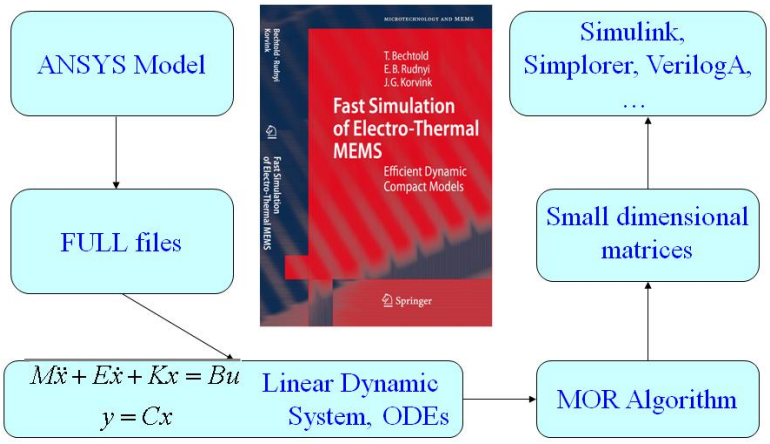

Fig. 1. The structure of MOR for ANSYS

3 Short Summary of the Previous Work

The main idea of our previous work [1] is expressed in Fig. 2. The thermal model of Freescale eXtream Switch devices has been developed in ANSYS with about 300.000 degrees of freedom. This gives us a reasonably accurate linear model however the transient simulation is out of reach from the viewpoint of system simulation. Four power transistors in the chip have been defined as independent power sources (four input functions in Eq. 3) and four junction temperatures have been defined as outputs. The reduced system of dimension 60 (15 degrees of freedom per input) approximates the original high dimensional ANSYS model with accuracy better than 1% and has been used in the electro-thermal simulation at the system level. Typical simulation results are presented in Fig. 3.

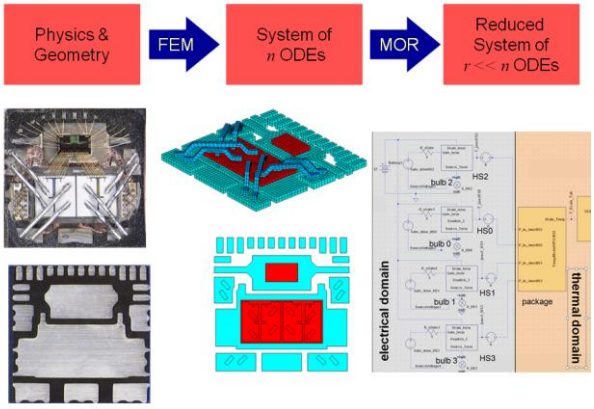

Fig. 2. From a finite element thermal model to electro-thermal simulation at the system level

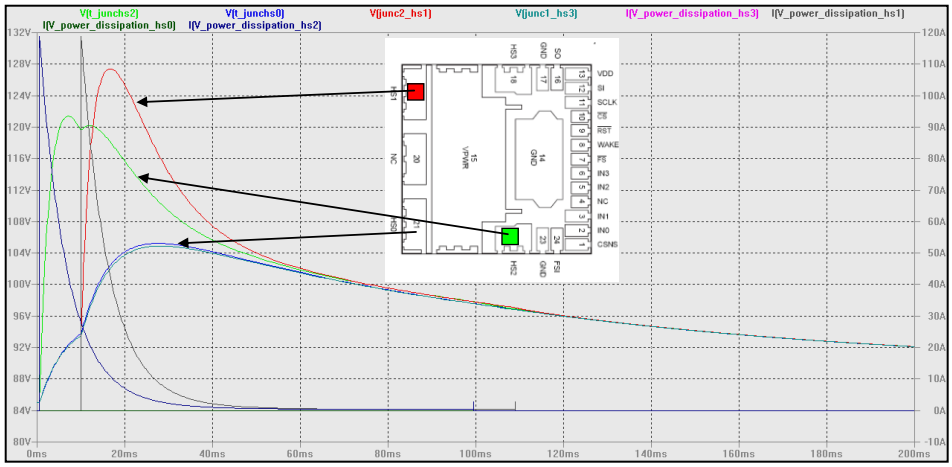

Fig. 3. Typical simulation results using SPICE [1]

4 Design Flow to Use Model Reduction

The implementation of the Arnoldi Algorithm (MOR for ANSYS) that was employed to generate the reduced model as shown in Fig 2 is a command-line tool. As a result, it is very straightforward to integrate in a custom design flow. In this section, we present how it this has been done in the case of ANSYS Workbench and Simplorer.

Fig 4 displays the package with two power transistors (Fig 4, a) and its half-symmetry model in ANSYS Workbench (Fig 4, b). Then the chip is shown on the PCB (Fig 4, c) and the thermal analysis in Workbench has been performed for this model. A typical temperature distribution is shown on the right in Fig 4, d.

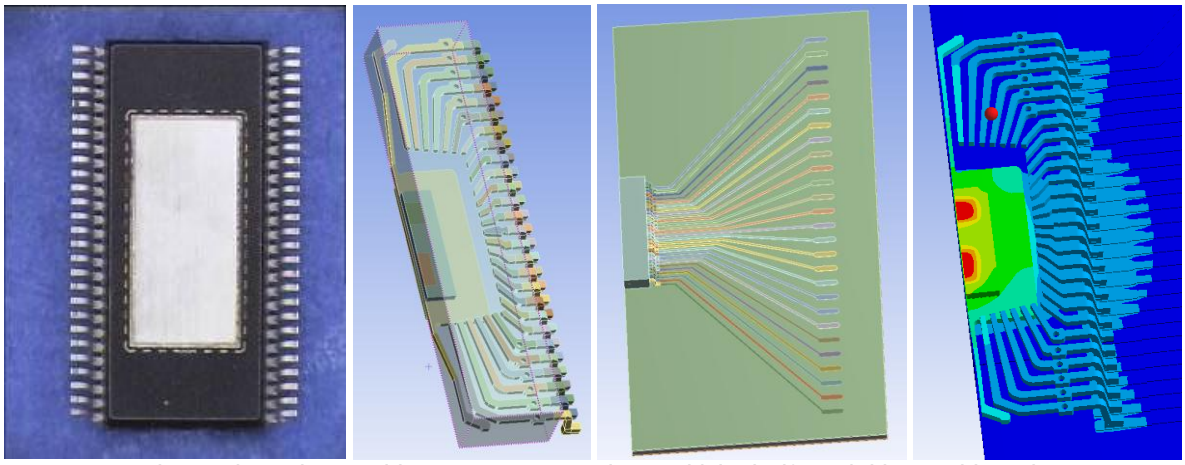

Fig. 4. a) Package with two power transistors; b) its half model in Workbench
c) the half model on a PCB d) the temperature distribution without the mold.

Once the model in Workbench is ready, a user defines so-called “named selections” to specify objects where power dissipation occurs. Then he/she inserts a command snippet that takes this information as input. The script is generic and only its arguments change from model to model. The script defines inputs as 1 W power dissipation per named selection and then defines the temperature outputs in the middle of defined surfaces (typically on the top of the die). This way the user can execute the model reduction directly from within the GUI of ANSYS Workbench.

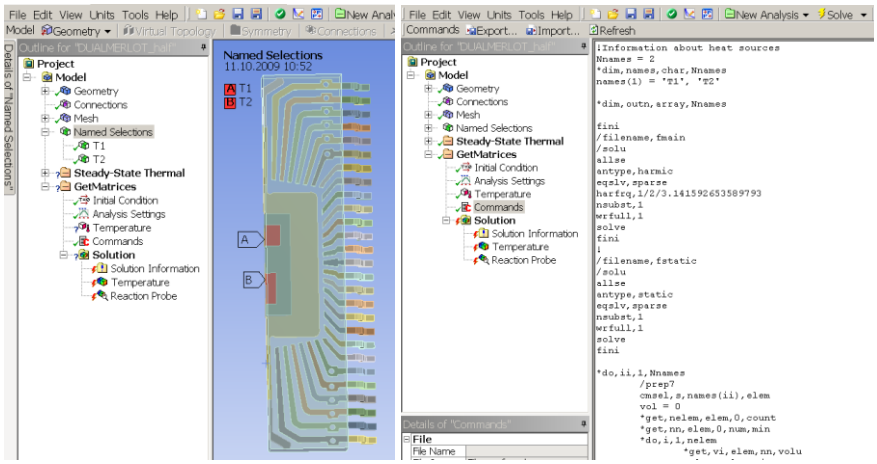

Fig. 5. Named Selections in Workbench (only chip is shown) and the command snippet that uses them to prepare information necessary for MOR for ANSYS

MOR for ANSYS generates a reduced model in the state-space form of Eq. (4) which can be directly read in Simplorer (see Fig. 6). Simplorer allows us to model thermal subsystems (Fig. 7) where the reduced model will be treated as a subsystem in a conservative nodal formulation: temperature and heat loss as across and through variables respectively. The reduced system also has a terminal that allows us to define the ambient temperature. The thermal impedance for one power source computed in Simplorer with the reduced model is compared with the results computed in ANSYS in Fig. 8. The difference is less than one percent while the reduced model has the dimension 30 (15 degrees of freedom per input) and the original ANSYS model has about 300.000 degrees of freedom.

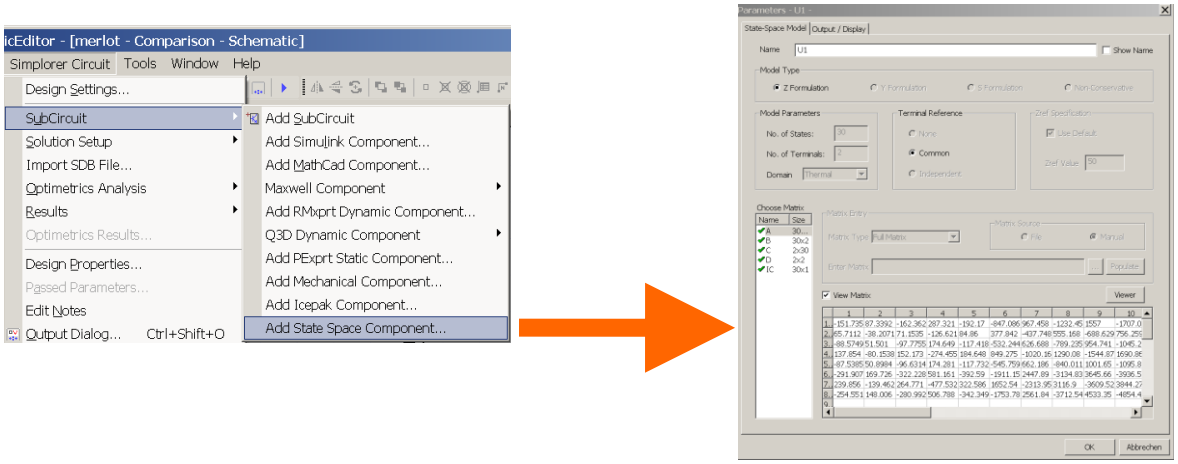

Fig. 6. Import of the reduced model in Simplorer

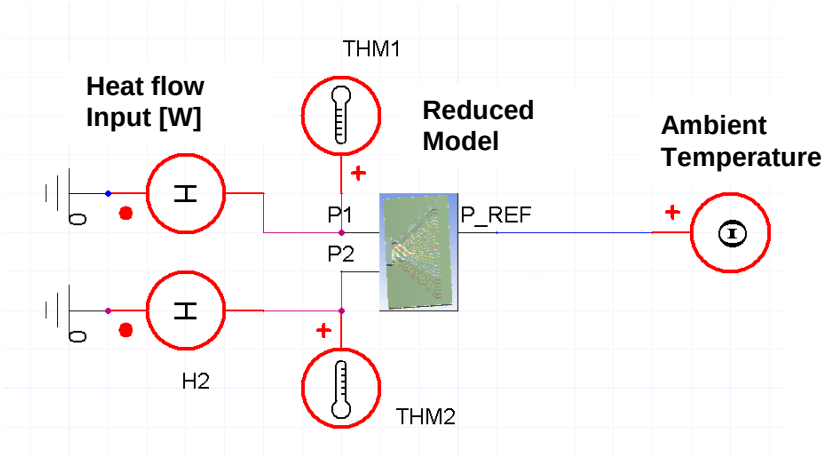

Fig. 7. Test circuit for the reduced model in Simplorer

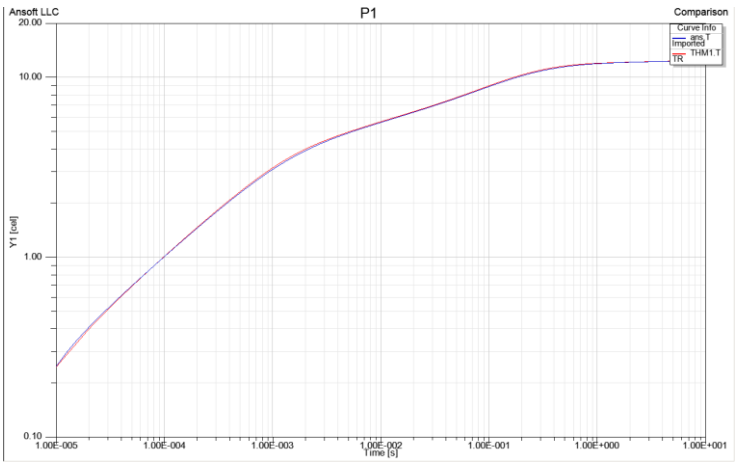

Fig. 8. Comparison of the thermal impedance of one transistor in Simplorer: the reduced model vs. the original ANSYS model

5 Thermal runaway

Thermal runaway refers to a situation where an increase in temperature changes the conditions in a way that causes a further increase in temperature leading to a destructive result. Let us demonstrate this phenomenon for the ohmic loss of a power transistor. We neglect any electrical transients and concentrate only onto the impact of the drain to source resistance at the on-state R_{DSon}, This resistance can be described as a linear function in the transistor junction temperature T_J:

$$R_{DSon} = R_0 + k(T_J - T_0)\,, \tag{5}$$

where R_0, k and T_0 represent the electrical resistance at a given reference temperature, the temperature coefficient and the reference temperature, respectively. The drain to source current I will cause heat generation of power P

$$P = I^2 R_{DSon} = I^2 R_0 + I^2 k(T_J - T_0)\,, \tag{6}$$

The heat generation will in turn result in a temperature rise, which depends on the ability of the structure to transfer the heat away from the transistor junction into the ambient environment. Let us consider a simple thermal model of one single heat path with the thermal resistance Θ_{JA} and one time constant τ. The heat transfer can be modeled by one equivalent thermal RC cell. The heat generation power P represents the net flux, whereas junction and ambient temperatures, T_J and T_A, represent the potentials in the opposite nodes of the RC-cell (Fig. 9).

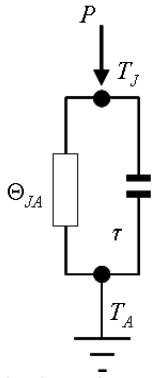

Fig. 9. Equivalent thermal RC-cell

The junction temperature is then determined by the following differential equation:

$$\frac{1}{\Theta_{JA}}\left(T_J - T_A\right) + \frac{\tau}{\Theta_{JA}}\frac{d}{dt}\left(T_J - T_A\right) = P\,. \tag{7}$$

Assuming a constant ambient temperature, replacing the heat generation power with (6) and re-arranging equation (7) finally yields the differential equation for the junction temperature as follows:

$$T_J\left(-\Theta_{JA} I^2 k\right) + \tau\frac{dT_J}{dt} = \Theta_{JA} I^2\left(R_0 - k\,T_0\right) + T_A\,. \tag{8}$$

By applying an integrating factor, equation (8) transforms into the next differential equation

$$\frac{d}{dt}\left(T_J e^{\left(\frac{1-\Theta_{JA} I^2 k}{\tau}t\right)}\right) = \frac{1}{\tau}\left(\Theta_{JA} I^2\left(R_0 - k\,T_0\right) + T_A\right) e^{\left(\frac{1-\Theta_{JA} I^2 k}{\tau}t\right)} \tag{9}$$

that can be integrated as follows:

$$T_J = e^{\frac{-1+\Theta_{JA} I^2 k}{\tau}t}\,\frac{1}{\tau}\left[\int\left(\Theta_{JA} I^2\left(R_0 - k\,T_0\right) + T_A\right) e^{\left(\frac{1-\Theta_{JA} I^2 k}{\tau}t\right)} dt + C_0\right], \tag{10}$$

with the integration constant C_0. We now assume that the junction temperature is equal to the ambient temperature at the initial state. Furthermore we assume a step function for the drain-source current I. The final solution for the junction temperature will then read

$$T_J = \frac{\Theta_{JA} I^2\left(R_0 - k\,T_0\right) + T_A}{1 - \Theta_{JA} I^2 k}\left(1 - e^{\frac{-1+\Theta_{JA} I^2 k}{\tau}t}\right) + T_A\, e^{\frac{-1+\Theta_{JA} I^2 k}{\tau}t} \tag{11}$$

If we set the temperature coefficient k to "0", we receive the well known solution of the step response for a constant drain-source on-resistance:

$$T_J = \Theta_{JA} I^2 R_0\left(1 - e^{\frac{-t}{\tau}}\right) + T_A\,, \tag{12}$$

but if the temperature coefficient *k* remains nonzero we will be able also to find an unstable condition for the junction temperature at a critical current value of

$$I_{cr} = \frac{1}{\sqrt{\Theta_{JA} k}} . \qquad (13)$$

The arguments of the exponential functions in (11) become positive for current values greater than the critical value, which causes the junction temperature to go to infinity with increasing time. Hence, the self-heating of the transistor will in these cases

$$I \geq I_{cr}, \quad t \to \infty, \quad T_J = \infty . \qquad (14)$$

always result in a thermal runaway phenomenon.

Fig. 10 shows the junction temperature rise as a function of time for different drain-source current to critical current ratios. All curves up to the ratio lower than the critical values of "1" reveal a finite steady state temperature. Curves with the ratio greater than or equal to "1" always result into a thermal runaway.

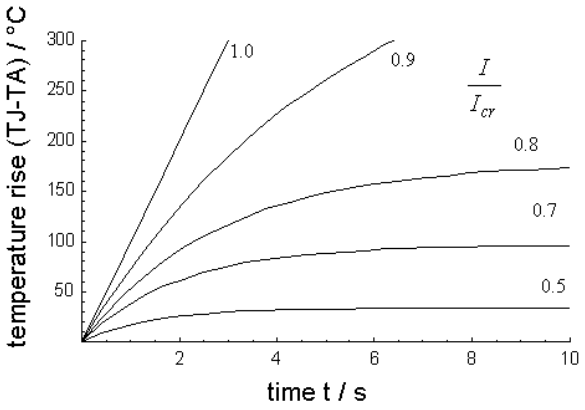

Fig. 10. Junction temperature rise over time and drain-source current to critical current ratio

6 Electro-thermal System Simulation

In this section we will demonstrate the phenomenon of thermal runaway for the Freescale semiconductor device introduced in Section 4 with two power transistors integrated on a single chip. The chip was assembled onto the exposed copper flag of a SOIC-type package. The copper flag is directly attached to a printed circuit board with thermal vias and heat spreading elements. Electrical and thermal domains are represented by separate behavioral models. The coupling of thermal and electrical domains and the system simulation of use cases will be achieved by means of the SIMPLORER tool.

As discussed above, the thermal behavior of power transistors driving an arbitrary load is dependent on a number of parameters. The main parameters being the thermal impedance of the cooling system, the ambient temperature T_A, the electrical dynamics of the load, and the parameters of R_{DSon}: k, R_0, T_0 from (5). We demonstrate the consequences of these dependencies through two case studies involving the compact thermal model of the chip:

1) DC current excitation
2) Transient turn on of automotive light-bulbs

The numerical study of the complete system behavior requires a "system simulation" combining the thermal dynamics of the transistor device and its environment with the electrical network equations of the power supply, transistor, and load. To this end, the system simulator Simplorer is used.

The R_{DSon} characteristic was implemented in the VHDL-AMS language, and features two electrical terminals for the drain-source current, and one thermal terminal for heat flow into the heat-sink. Fig. 11 shows the code for this model, corresponding to (4)

```
LIBRARY IEEE;
USE IEEE.ELECTRICAL_SYSTEMS.ALL;
USE IEEE.THERMAL_SYSTEMS.ALL;

ENTITY RDS_MODEL IS
   PORT (        QUANTITY RDS1 : RESISTANCE := 0.035;
                 QUANTITY t0 : IN TEMPERATURE := 298.0;
                 QUANTITY KC1 : REAL := 0.35e-3;
                 QUANTITY CTRL: REAL := 0.0;
                 TERMINAL th1 : thermal;
                 TERMINAL p,m  : ELECTRICAL);
END ENTITY RDS_MODEL;

ARCHITECTURE behav OF RDS_MODEL IS
                 QUANTITY v ACROSS i THROUGH p TO m;
                 QUANTITY t_val ACROSS h THROUGH th1 TO thermal_ref;
BEGIN
        IF (CTRL <= 0.0) USE
                 i == 0.0;
                 h == 0.0;
        ELSE
                 v == i*(RDS1+KC1*(t_val-t0));
                 h == -i*v;
        END USE;
END ARCHITECTURE behav;
```

Fig. 11. VHDL-AMS Model of the temperature-dependent drain – source resistance.

6.1 Case Study 1: DC loading of the MOSFET

The case of the DC excitation can be used to determine the critical steady-state current above which thermal runaway will occur. Fig 12 shows the simple Simplorer model used for this calculation. In Simplorer, the A, B, C matrices of the reduced-order model of the chip thermal model are read in directly using the built-in multi-domain state-space model. The transistor was modeled as a temperature dependent thermal resistor with the VHDL_AMS representation from Fig. 11. For this test, one transistor is supplied with DC current, while the other is disconnected. The Power P dissipated across R_{DSon} is injected into the thermal network. The conservative formulation ensures that both electrical and thermal equations are solved simultaneously for a closed electro-thermal solution.

Fig. 13 shows the results of the junction temperature T_J of the transistor under test assuming ambient temperature of 25°C. It can be seen that the critical current is about 20 A. Fig 14 shows the maximum temperature reached after 100 ms DC excitation for ambient temperatures of 25°C, 50°C and 75°C. Here it is apparent that the critical current is also dependent to a certain extent on the ambient temperature. These dependencies indicate the importance of a coupled electro-thermal simulation in obtaining reliable results.

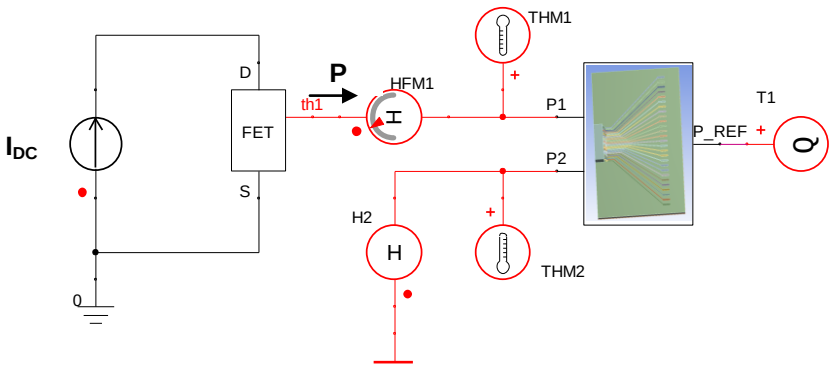

Fig. 12. DC test circuit modeled in Simplorer

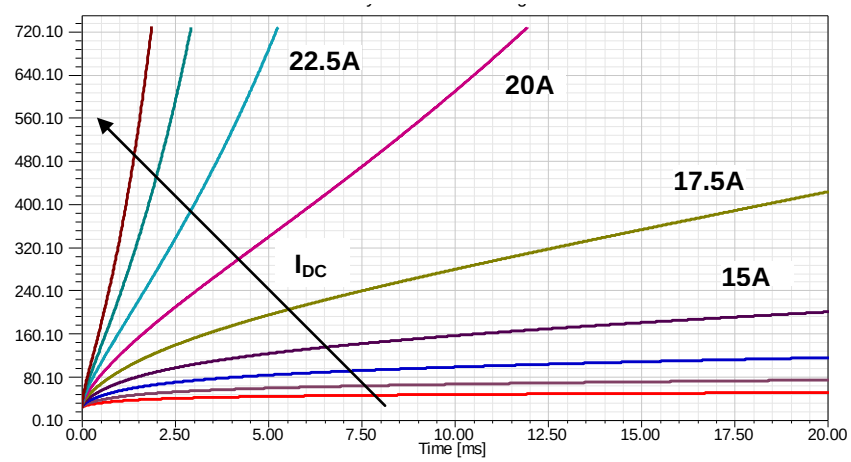

Fig. 13. Transient junction temperature curves as a function of dc loading level
T_A = 25°, k = 3.5e-4, R_0 = 35mOhm, T_0 = 25°C,

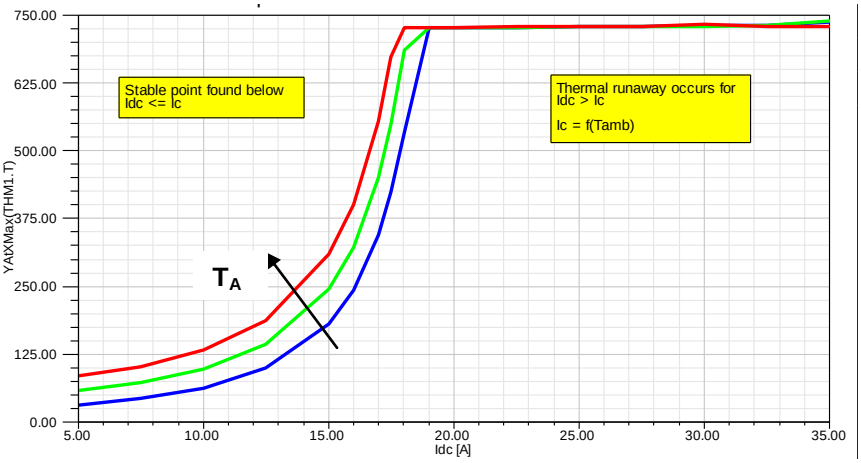

Fig. 14. Maximum junction temperature @ t = 100ms vs. dc loading level for ambient temperatures 25°C – 75°C k = 3.5e-4, R_0 = 35mOhm, T_0 = 25°C.

6.2 Case Study 2: Transient Turn-on of an Automotive Light-Bulb

In this case, the MOSFET is to be used to drive an automotive light-bulb of type P21W. The light-bulb model is represented using an existing Spice model which was imported directly into Simplorer. The test considers the turn-on characteristics of the circuit considering 1, 2, or 3 bulbs in parallel (see Fig 15). Fig. 16 shows the transient current waveforms for these cases. The maximum current and steady-state currents increase more or less proportionally to the number of bulbs. Fig. 17 shows the transient behavior of T_J for the three loading cases. It is apparent that the temperature increases non-linearly with the loading level due to the thermal runaway phenomenon.

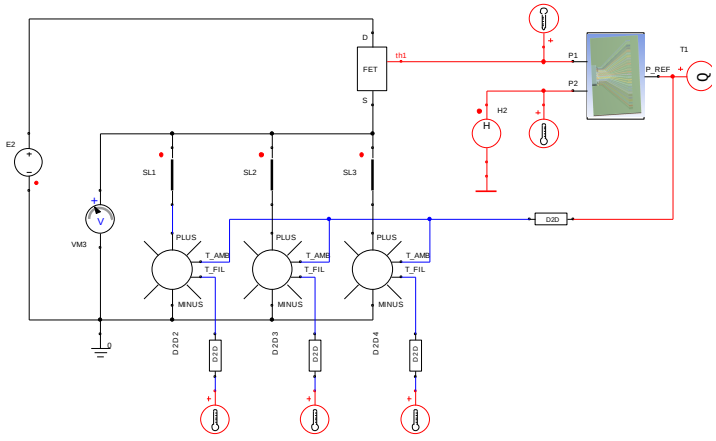

Fig. 15. Simulation model of P21W light-bulb use case

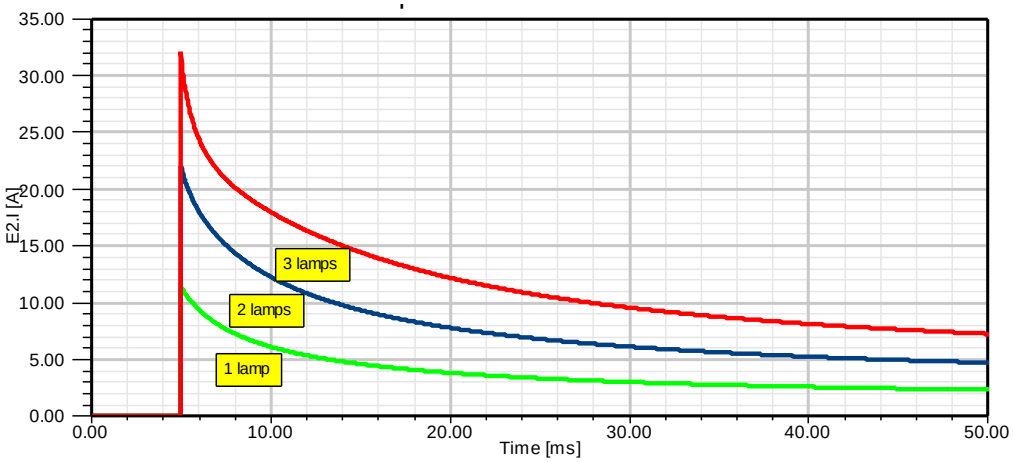

Fig. 16. Transistor currents vs. time as a function of number of lamps
T_A = 25°, k = 3.5e-4, R_0 = 35 mOhm, T_0 = 25°C,

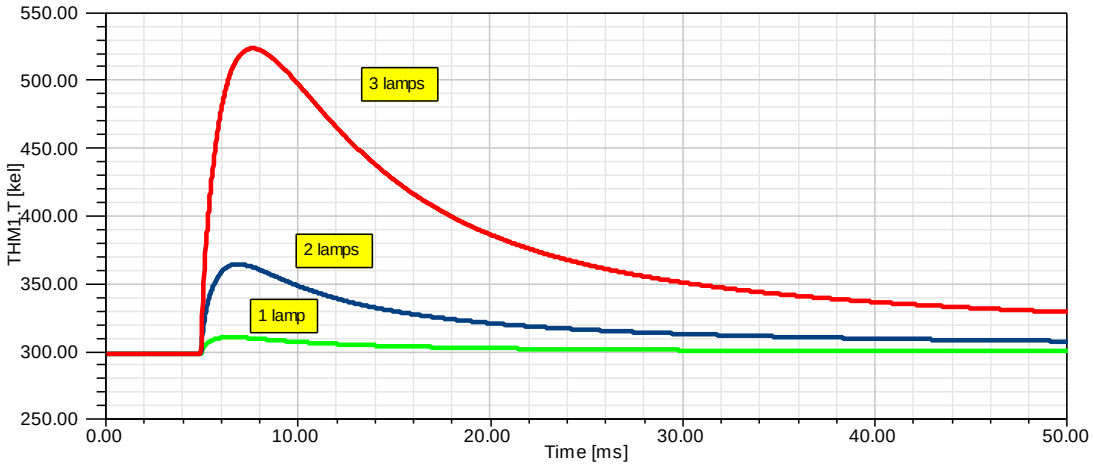

Fig. 17. T_J vs. time as a function of number of lamps
T_A = 25°, k = 3.5e-4, R_0 = 35mOhm, T_0 = 25°C.

7 References

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